PHILADELPHIA SECTION of the IEEE

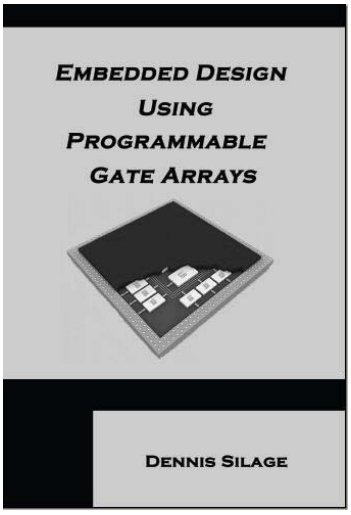
Almanack

Successful FPGA Class

By Mark Soffa

On two successive Fridays, October 17 and 24, 2008, a group of 15 EEs joined Dr. Dennis Silage at his EE Lab at Temple University to attend the IEEE Philadelphia Section's *Embedded Design Using Programmable Gate Arrays* Short Course. I had heard about FPGAs (Field Programmable Gate Arrays) for years, and I knew that EEs no longer built systems with 7400 logic; but I didn't know how easy it was to implement programmable logic with the new tools such as the Verilog language.

The learning environment was perfect! We each had a PC preloaded with the latest Xilinx development environment, our very own Digilent development board, complete with a Xilinx Spartan 3E FPGA, and enough peripherals to do some interesting stuff. We also didn't sit for hours in front of a blackboard. Instead, Dr. Silage lectured about the Verilog language for a while and right away we were each on our PCs looking at FPGA code and learning what it takes to implement a SPI (serial peripheral interface). By mid-morning, the SPI bus was running on our development board, and light emitting diodes were flashing.



The class was structured with a series of short lectures followed by labs to lock in the concepts. For the next day and a half we covered many of the topics in Dr. Silage's book *Embedded Design Using Programmable Gate Arrays* and did two in-class projects. We created some advanced features (advanced for us, that is) by implementing a stopwatch on the development board's LCD. We all learned a lot and emerged from the class fired up!