

# EE3623 Embedded System Design Laboratory

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## Controller-Datapath in Verilog

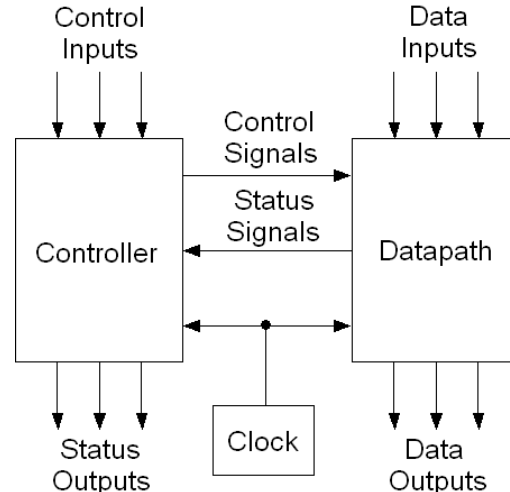
In this Laboratory you will be introduced to the implementation of the controller-datapath paradigm in Verilog. Controllers and datapath are important design elements in complex processes in embedded system design.

The Xilinx ISE projects for the liquid crystal display (LCD) are listed on pages 121-131 of the *Embedded System Design using Programmable Gate Array* text.

The project specifications are to output a signed 3-digit BCD number in the range  $\pm 999$  at line 2 position 5 of the LCD. The positive (+) and negative sign (-) is to be displayed on the LCD.

The signed 3-digit BCD number must suppress *leading zeros*. For example: -012 is to be properly displayed as - 12 with one leading space and +000 as + 0 with two leading spaces.

The 3-digit BCD number is inputted with the rotary shaft encoder. The ROTCTR pushbutton resets the number to +000. The number is incremented with a clockwise rotation of the rotary shaft encoded (ROTA) or decremented with a counter clockwise rotation of the rotary shaft encoded (ROTB). The *debounced* rotary shaft encoder signals should be used for smooth operation which requires the *clock.v* module.



The EAST and WEST pushbuttons (PB) provide coarse adjustment of the incrementation or decrementation of the signed 3-digit BCD number. The EAST pushbutton causes the BCD number to increment or decrement by 10 for each rotary shaft encoder signal while the WEST pushbutton does the same but with a factor of 50. The *debounced* pushbutton design reuse module *pbdebounce.v* should be used for smooth operation which requires the *clock.v* module.

The task of the Laboratory is to develop controller-datapath Verilog modules to accomplish the specification. The control input to the controller is the ROTCTR,

EAST PB and WEST PB signal and the data inputs to the datapath are the ROTA and ROTB from the *rotary.v* module (not shown) as a *design reuse*.

The datapath configures the signed 3-digit BCD data for display on the LCD as data outputs but provides only status signals to the controller and no control signal to any other module including *lcd.v* as the strict definition of a datapath.

The data outputs of the datapath are inputted to the LCD module *lcd.v* as design reuse. There are control signals from the controller to the LCD module and status return signals from the LCD module.

It would be a reasonable part of the design process to sketch (neat hand drawing is acceptable) the complete configuration of the design reuse modules and the controller(s) and datapath(s) as in the elapsed time project Figure 3.4 of the text and include that in your project report.

The complete project is to be implemented as a top module with nested modules including the design reuse modules and the controller(s) and datapath(s).

Although a rather large single module can be configured for this task, the project may not be synthesizable. The Laboratory is to introduce the controller-datapath concept and no other solution will be accepted.



This is a *two week* Laboratory for February 12th and 19th and the project report due date is February 26th.

You must demonstrate your project to the Teaching Assistant or to the Instructor and submit this Laboratory initialed with your completed Laboratory report.

Project Completion \_\_\_\_\_ (TA or I)  
Date \_\_\_\_\_

Spring 2009

